US008487658B2

(12) **United States Patent**
Datta et al.

(10) **Patent No.: US 8,487,658 B2**
(45) **Date of Patent: Jul. 16, 2013**

(54) **COMPACT AND ROBUST LEVEL SHIFTER LAYOUT DESIGN**

(75) Inventors: **Animesh Datta**, San Diego, CA (US); **William James Goodall, III**, Cary, NC (US)

(73) Assignee: **QUALCOMM Incorporated**, San Diego, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 79 days.

(21) Appl. No.: **13/180,598**

(22) Filed: **Jul. 12, 2011**

(65) **Prior Publication Data**

US 2013/0015882 A1 Jan. 17, 2013

(51) **Int. Cl.**
H03K 19/00 (2006.01)
H01L 25/00 (2006.01)

(52) **U.S. Cl.**
USPC **326/101**; 326/80; 326/63; 257/206

(58) **Field of Classification Search**
None
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,780,881	A	7/1998	Matsuda et al.	
6,414,518	B1	7/2002	Patel et al.	
6,974,978	B1 *	12/2005	Possley	257/204
7,095,063	B2	8/2006	Cohn et al.	
7,408,269	B2	8/2008	Joshi et al.	
2003/0231046	A1	12/2003	Giacomini et al.	
2004/0225985	A1	11/2004	Kashiwagi et al.	
2008/0143418	A1	6/2008	Lu et al.	
2008/0265936	A1	10/2008	Vora	
2009/0108904	A1	4/2009	Shiffer, II	
2010/0214002	A1	8/2010	Miyoshi et al.	
2010/0238744	A1	9/2010	Yano	
2011/0001538	A1	1/2011	Alam	
2011/0031944	A1 *	2/2011	Stirk et al.	323/234
2011/0266631	A1 *	11/2011	Morino et al.	257/371

FOREIGN PATENT DOCUMENTS

JP	2008067411	A	3/2008
WO	2006025025	A1	3/2006

OTHER PUBLICATIONS

International Search Report and Written Opinion—PCT/US2012/046562—ISA/EPO—Sep. 24, 2012.

* cited by examiner

Primary Examiner — Jany Richardson
(74) *Attorney, Agent, or Firm* — Sam Talpalatsky; Nicholas J. Pauley; Joseph Agusta

(57) **ABSTRACT**

Method and apparatus for voltage level shifters (VLS) design in bulk CMOS technology. A multi-voltage circuit or VLS that operate with different voltage levels and that provides area and power savings for multi-bit implementation of level shifter design. A two-bit VLS to shift bits from a first voltage level logic to a second voltage level logic. The VLS formed with a first N-well in a substrate. The VLS formed with a second N-well in the substrate, adjacent to a side of the first N-well. The VLS formed with a third N-well in the substrate, adjacent to a side of the first N-well and opposite the second N-well. A first one-bit VLS circuit having a portion formed on the first N-well and a portion formed on the second N-well. A second bit VLS circuit having a portion formed on the first N-well and a portion formed on the third N-well.

23 Claims, 5 Drawing Sheets

Compact physical design of 2-bit shifter layout